What is claimed is:

1. An integrated semiconductor memory chip comprising:

hardwired presence detect data which can be accessed for transmission to a location external to the memory chip; and

logic allowing additional presence detect data to be programmed in the memory chip after fabrication of the memory chip.

2. The memory chip of claim 1 wherein the hardwired presence detect data includes a plurality of bits, wherein a value of each hardwired bit is based on whether a conductive region of the chip corresponding to that bit is connected electrically to a predetermined voltage when power is supplied to the chip.

3. The memory chip of claim 2 wherein the value of each hardwired bit is based on whether the conductive region of the chip corresponding to that bit is connected electrically to ground.

4. The memory chip of claim 2 wherein a difference between a first hardwired bit representing a digital high value and a second hardwired bit representing a digital low value is the presence or absence of a portion of a metal layer.

5. The memory chip of claim 2 wherein a difference between a first hardwired bit representing a digital high value and a second hardwired bit representing a digital low value is the presence or absence of a portion of a polysilicon layer.

6. The memory chip of claim 2 wherein a difference between a first hardwired bit representing a digital high value and a second hardwired bit representing a digital low value is the presence or absence of doping in a portion of a semiconductor substrate on which the memory chip is fabricated.

7. The memory chip of claim 1 wherein the logic allowing additional presence detect data to be programmed in the memory chip after fabrication of the memory chip includes a programmable fuse corresponding to each bit of programmable presence detect data.

8. The memory chip of claim 7 wherein the programmable fuse is an antifuse.

9. The memory chip of claim 7 wherein the programmable fuse is a laser fuse.

10. The memory chip of claim 7 wherein the programmable fuse is an electrical fuse.

11. The memory chip of claim 1 wherein the logic allowing additional presence detect data to be programmed in the memory chip after fabrication of the memory chip includes a flash transistor corresponding to each bit of programmable presence detect data.

12. An integrated semiconductor memory chip comprising:

hardwired presence detect data;

logic allowing additional presence detect data to be programmed in the memory chip after fabrication of the memory chip;

a counter for receiving a control signal and for providing address bits at its output in response to the control signal; and

a switching device for allowing the presence detect data to be selected individually in response to the address bits for serial transmission to a location external to the memory chip.

13. The memory chip of claim 12 wherein the switching device includes a multiplexer.

14. The memory chip of claim 12 wherein the switching device includes a cascade of transistors.

15. A memory module comprising:

a plurality of memory chips, wherein at least one of the memory chips includes:

presence detect data which can be accessed for transmission to a location external to the memory module.

16. The memory module of claim 15 wherein the presence detect data includes a plurality of bits and wherein a difference between a first bit representing a digital high value and a second bit representing a digital low value is the presence or absence of a corresponding conductive region connected electrically to a predetermined voltage when power is provided to the chip.

17. The memory module of claim 15 wherein each of the memory chips has a same memory capacity.

18. The memory module of claim 15 wherein the memory chips include dynamic random access memory chips.

19. The memory module of claim 15 wherein the at least one memory chip includes:

a counter for receiving a control signal and for providing address bits at its output in response to the control signal; and

a switching device for allowing the presence detect data to be selected individually in response to the address bits for serial transmission to a location external to the memory module.

20. The memory module of claim 19 wherein the switching device includes a cascade of transistors.

21. A computer system comprising:

a central computer unit for supplying a memory address;

a memory controller for converting a memory address supplied by the central processing unit into address and control signals for accessing a memory location in a memory module and for transmitting presence detect data to the central processing unit;

a memory module including:

drivers for receiving the address and control signals; and

a plurality of memory chips, wherein at least one of the memory chips includes presence

detect data which can be accessed for transmission to the memory controller.

22. The computer system of claim 21 wherein the presence detect data includes a plurality of bits, and wherein the at least one memory chip includes:

a counter for receiving a control signal initiated by central processing unit and for providing address bits at its output in response to the control signal; and

a switching device for allowing the presence detect bits to be selected individually in response to the address bits for serial transmission to memory controller.

23. A method of providing information relating to configuration of a memory device, the method comprising:

hardwiring a first set of presence detect bits on an integrated semiconductor memory chip during fabrication of the memory chip.

24. The method of claim 23 wherein the act of hardwiring includes using a mask programmable photolithographic pattern.

25. The method of claim 23 further including:

providing a second set of programmable presence detect bits on the memory chip.

26. A method of providing information relating to a configuration or capabilities of a memory device comprising an integrated semiconductor memory chip with a set of programmable presence detect bits on the memory chip, the method including:

setting a value for at least one of the programmable presence detect bits.

27. The method of claim 26 wherein setting a value for the at least one presence detect bit includes:

applying a voltage across an antifuse on the memory chip to form a short circuit.

28. The method of claim 26 wherein setting a value for the at least one presence detect bit includes:

directing radiation at a fuse on the memory chip to form an open circuit.

29. The method of claim 26 wherein setting a value for the at least one presence detect bit includes:

raising a turn-on threshold voltage level of a transistor on the memory chip.

30. The method of claim 29 wherein raising the turn-on threshold voltage includes applying a voltage across a drain and control gate of the transistor so as to trap charge in a floating gate of the transistor.

31. A method of providing information relating to configuration or capabilities of a memory module comprising at least one integrated semiconductor memory chip, the method comprising:

accessing presence detect data stored on the at least one memory chip; and

sending the presence detect data to a memory controller.

32. The method of claim 31 further including sending the presence detect data from the memory controller to a central processing unit.

33. The method of claim 31 wherein the presence detect data is sent to the memory controller in serial form.